REMARKS

In response to the Office Action, claims 1, 19, 21, 23 and 24 have been amended. New claims 34-41 have been submitted for the Examiner's consideration. Accordingly, claims 1-41 are currently pending.

Claims 1-3, 7, 8, and 21-23 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,242,348 to Kamal et al.

Amended claim 1 recites a method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of (a) forming a metal film on a semiconductor layer of a substrate, and (b) performing a first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer. Next, in step (c) an unreacted portion of the metal film is removed after the step (b). Thereafter,(d) impurity ions are implanted into the first silicide film so as to change the first silicide film into an amorphous second silicide film. In step (e) second thermal annealing is performed to change the amorphous second silicide film into a polycrystalline third silicide film, the third silicide film being at least a part of the member.

Amended claim 21 recites a method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of (a) forming a metal film on a semiconductor layer of a substrate; and (b) performing a first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer. Next, in step (c) an unreacted portion of the metal film is removed after the step (b). In step (d), nitrogen is introduced into the semiconductor layer in a step after the step (a) and before the step (c). After the step (d), a second thermal annealing is performed to change the first silicide film into a second silicide film, the second silicide film being at least a part of the member.

Due to the method of the present invention partial interruptions are unlikely to occur in the final silicide film making it possible to form the third silicide film as a single, continuous film having a uniform thickness. See, the specification at page 25, lines 8-11. Accordingly, the disruption of the silicide film and the occurrence of uneven thickness due to agglomeration can be prevented.

In contrast, Kamal teaches the steps of forming a cobalt silicide (CoSi) layer 122, 124 by performing a first thermal annealing; implanting boron and nitrogen into a substrate on which the cobalt silicide layer is formed; and thereafter, forming a cobalt silicide ($CoSi_2$) layer 132, 134 by performing a second thermal annealing.

Kamal does not disclose or suggest the step of "performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer" as recited in amended claims 1 and 21. Nor, does Kamal disclose or suggest Kamal's cobalt silicide layer 122,124 is not a silicide layer rich in cobalt.

Moreover, Kamal does not disclose or suggest the step of "(d) introducing nitrogen into the semiconductor layer in a step after the step (a) and before the step (c), as recited in claim 21. Hence, according to amended claim 21, nitrogen is introduced into the substrate layer *before* removing the unreacted portion of the metal film. Kamal, oppositely, discloses implanting nitrogen *after* removing the unreacted portion of the cobalt film.

Accordingly, as set forth above, Kamal does not disclose or suggest the claimed subject matter. Therefore, claims 1-3, 7-8 and 21-23 are allowable over Kamal.

Claim 9 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamal in view of U.S. Patent No. 5,659,194 to Iwamatsu et al.

Iwamatsu fails to cure the deficiencies of Kamal as Iwamatsu does not disclose or suggest "performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer" as recited in amended claims 1 and 21.

Claim 19 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamal in view of U.S. Patent No. 5,659,194 to Frenkel et al.

Amended claim 19 recites a method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of (a) forming a metal film whose main component is cobalt on a semiconductor layer of a substrate; and (b)

performing a first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first cobalt silicide film that is rich in cobalt on the semiconductor layer. Next, in step (c) an unreacted portion of the metal film is removed after step (b). In step (d), a second thermal annealing is performed after step (c) at a temperature of 725°C or less to change the first cobalt silicide

film into a second cobalt silicide film, the second cobalt silicide film being at least a part of the member.

Frenkel, like Kamal, does not disclose or suggest "performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first cobalt silicide film that is rich in cobalt on the semiconductor layer," as recited in amended claim 19.

As none of the cited prior art, either alone or in combination, discloses or suggests the claimed subject matter, claims 19, 20, 23 and 24 are allowable.

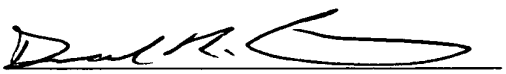
Claim 24 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Kamal and further in view of U.S. Patent No. 5,627,105 to Delfino et al. and U.S. Patent No. 4,701,349 to Koyanagi et al.

Neither Delfino nor Koyanagi disclose or suggest "performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first cobalt silicide film that is rich in cobalt on the semiconductor layer," as recited in amended claim 19.

Therefore, claim 24 is also allowable over the cited prior art.

Given the above, none of the cited prior art discloses or suggests the claimed subject matter. Therefore, Applicant's respectfully submit that the application is now in condition for allowance. A prompt passage to issuance is therefore earnestly solicited.

Respectfully submitted,



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MARKED UP VERSION

1. (Amended) A method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of:

(a) forming a metal film on a semiconductor layer of a substrate;

(b) performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer;

(c) removing an unreacted portion of the metal film after the step (b);

(d) implanting impurity ions into the first silicide film so as to change the first silicide film into an amorphous second silicide film;

(e) performing second thermal annealing to change the amorphous second silicide film into a polycrystalline third silicide film, the third silicide film being at least a part of the member.

19. (Amended) A method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of:

(a) forming a metal film whose main component is cobalt on a semiconductor layer of a substrate;

(b) performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first cobalt silicide film that is rich in cobalt on the semiconductor layer;

(c) removing an unreacted portion of the metal film after the step (b); and

(d) after the step (c), performing second thermal annealing at a temperature of 725°C or less to change the first cobalt silicide film into a second cobalt silicide film, the second cobalt silicide film being at least a part of the member.

21. (Amended) A method for manufacturing a semiconductor device including a member which is partially silicified, comprising the steps of:

(a) forming a metal film on a semiconductor layer of a substrate;

(b) performing first thermal annealing to cause a silicification reaction between the metal film and the semiconductor layer so as to form a polycrystalline first silicide film that is rich in metal on the semiconductor layer;

(c) removing an unreacted portion of the metal film after the step (b);

(d) introducing nitrogen into the [first silicide film before, in, or after, any of the steps (a) to (c)] semiconductor layer in a step after the step (a) and before the step (c); and

(e) after the step (d), performing second thermal annealing to change the first silicide film into a second silicide film, the second silicide film being at least a part of the member.

23. (Amended) The method for manufacturing a semiconductor device of claim [19] 21, wherein the semiconductor layer is a part of a source/drain region of a MISFET, the method further comprising, before the step (a):

a step of forming a gate insulative film and a gate electrode on an active region including the semiconductor layer;

a step of forming an insulative side wall on a side surface of the gate electrode; and

a step of forming a source/drain region by implanting impurity ions into each of portions of the active region on both sides of the gate electrode and then activating the impurity, wherein the step (d) is performed after the step of forming a source/drain region and before the step (a).

24. (Amended) The method for manufacturing a semiconductor device of claim [19] 21, further comprising a pre-cleaning step of irradiating a surface of the semiconductor layer with plasma before the step (a), wherein the step (d) is performed by introducing nitrogen-containing plasma in the pre-cleaning step.